1st 300KV Marx

High Voltage Power Supply

Eliminate Sustained Arc



L1 / Circuit Removed



Circuit Board Bottom View







Waveforms of U1 - 3 / Circuit board only => not connected to Q1



(U2 pin 3) triggers U1

which sets the duty cycle

Eliminate Sustained Arc

14 Feb. 01a

Transformer Example # 27-sep-99a (Note that the transformer used in this PS is labeled: 4 Oct 99 and is not an exact copy)

Info from notebook 4 Oct. 99:

- core

- ferrite from computer PS transformer (no markings on core). .. Appears to be type 3E8

- primary $10T \Rightarrow 20$ gauge
- secondary 210T => 28 gauge
 - 0.75" E core top view <0.5" 0.25" 1.75" Side View



Gap set by one viewgraph sheet thickness



Eliminate Sustained Arc







Eliminate Sustained Arc

_ Typically have 40 - to - 43 T per layer & 5 layers to get \sim 210T for the secondary

Comment:

As mentioned previously many of the ferrite cores experimented with were obtained from PC switching PS. This involved removing the core from the winding which is very difficult to do. A limited number of used ferrites were used for the initial prototypes; as this supply diminished the above method was necessary. Consequently various transformers were constructed having various core size and types consequently U2 & 3 adjustments varied as well as performance.

- Another physical example (ferrite from PC switching PS):





Top View



Eliminate Sustained Arc







Waveform @ U2 pin 3

Flyback Counter EMF @ T1 primary

Comment: For some reason after re-installing the circuit the waveform timing has changed



Gate drive to IGBT used for driving Xformer #27sep-99a

volts







Waveforms when the output is loaded



Loss mechanisms believed to be due to: - core saturation - small Δt at peak (when not saturated) for 70nsec UF1007s

Possible improvements to increase efficiency - increase air gap in core - add caps @ primary & sec to increase width

Purpose:

The 2nd HVPS utilizing cyclic HV inhibit was initially tested, 12 Jan. 00, with a 16 stage Marx generator; the experimental setup is shown below:



Close up of HVPS:



Ch 2

1st Waveform Set:

$Vcharge \sim 18 KV$
V Marx ~ 280KV

Note: although U3 was initially set for 90 ms on and 10 ms off the actual PRF for self breakdown was ~ 8 hz.

18* 16 = 288

16 stages => 2700 pf/4= 675 pf/stage; equivalent C parallel = ~ 0.011 \mu f

(a) $18kv = 0.5(CV^2) = 1.782 J/pulse$

1.782J* 8hz =14.256 W

HVPS input current = $\sim 4.5 \text{A}$ @ $\sim 11.8 \text{V}$ =>53.1W 27% PWR in -to - PWR to Marx

Photos\ experimental setup another view



New 16 Stage Marx / Direct Output (no peaking gap) FN12JAN00A







2nd Waveform Set:



Waveform $\ Vch \ get PRF$:







Top diodes

Bottom diodes

Ea. Diode = 20 UZ1007 connected in series

Top view

Super glue together& line up



The HVPS was initially designed and tested in a modular component fashion to facilitate troubleshooting. For example the IGBT was tested with a transformer using a function generator as the gate drive (PRF and duty cycle); which was replaced with two 555s. When used with a Marx it was discovered that cyclic enable/inhibit was necessary to prevent troublesome sustained arcing; resulting in an additional 555. Since most of the component functional parameters have been determined it would appear that U1,2, &3 could be replaced with a single switching PS IC controller chip in a future design.

U2 Switching Frequency Osc. :

The active devices (U1,2,&3) used in the HVPS utilizes the 555 timer. Fig. 1 provides the pin out and Fig. 2 the functional block schematic. The two comparators have one of the sense inputs connected at 1/3 and 2/3 Vcc of the resistor divider 3R approximating the charge and discharge time constant (T=RC). Fig. 3 shows the 555 configured in osc. mode. The other comparator inputs (threshold & trigger) are used in the osc. timing; because the sense points are fixed (1/3 & 2/3 Vcc) the osc. frequency is independent of Vcc. The HVPS is designed to operate at 12VDC which is well within the maximum Vcc of ~ 16V.

The optimum operating switching frequency was experimentally determined to be in the 12 to 20Khz range. The value for $R_A + 2R_B$ was determined using Fig. 4 to be ~ in the 2 to 10K range for $C = 0.01 \mu f$. The frequency is given as:

$$F = \frac{1.44}{(R_A + 2R_B)}$$

To allow slack the low frequency was set at 10Khz for C fixed; hence:

$$R_{A} + 2R_{B} = \frac{1.44}{(1E4)(1E-8)} = 14.4K\Omega$$

and the high frequency at 50Khz:

$$R_A + 2R_B = \frac{1.44}{(5E4)(1E-8)} = 2.88K$$

For the 1st iteration if R_A varies from ~ 0 to 12K; then $2R_B = ~ 3K$; however some minimal R_A resistance is needed to protect and isolate the **discharge** from Vcc. If the upper frequency is reduced to ~ 20 to 30Khz then $R_A + 2R_B$ = ~ 6K.

$$D = \frac{R_{\rm B}}{R_{\rm A} + 2R_{\rm B}}$$

FREE RUNNING FREQUENCY vs R_A, R_B AND C



From the above equation to get trigger pulses from U2's output @ pin 3 some D value is required; hence a finite R_B is needed. The minimum value (that includes at least the pulse rise and fall time) was experimentally determined to be ~ 2K. The resultant circuit at the right indicates $R_B = R6 =$ 2.2K and $R_A = R5 + VR2$ Notes: HVPS\ NE555 Design U1,2, & 3

After much experimentation for the particular system application decision was made to operate the switching PS in a cyclic manner (enable/ inhibit). The PS would run full blast charging the Marx generator to a certain value (for self breakdown charge to this value); after firing the PS would be inhibited long enough for the plasma to die sufficiently so that no sustained arcing occurred. This investigator measured these parameters using an early free run representative prototype PS and Marx.

The diagrams at the right are from this investigators notebook in order to determine U3's duty cycle. The top indicated about 90msec to charge a representative 16 stage Marx bank. The DSO sweep was increased for viewing several msec/div resolution. Sustained SG arcing of the Marx was encouraged and discouraged in order to determine the plasma lifetime. The bottom expanded waveform drawing indicates that ~ 11msec inhibit is required. With these parameters at hand U3 components could be determined.

Design was started by letting $C = 1\mu f$ and free run frequency in the 5 - to - 10 hz range; @ 5hz:

$$R_{A} + 2R_{B} = \frac{1.44}{(5)(1E-6)} = 288K$$

(a) 10 hz
$$R_A + 2R_B = 144K$$

Copying the information from the notebook; the off time (T_2) was assumed to be conservatively 15 - to - 100msec. And an on time (T_1) of ~ 90msec. The equations for $T_1 \& T_2$ are given:

$$T_1 = 0.693(R_A + R_B)C$$
 $T_2 = 0.693(R_B)C$

 $T_2 = 15$ msec. = 0.693(R_B) 1µf => $R_B = 21.6$ K

 $T_1 = 144.3K$; total period $T = T_1 + T_2 = 0.693(R_A + 2R_B)C$

(a) 10 hz $R_a + 2(21.6E3) = 144E3 \implies R_A = \sim 100K$

 $R_{A} + R_{B} = \sim 122K$

(a) 5hz $R_A + 2R_B$ = 288K ; $R_B = 94K$

To simplify the design both R_A & .R_B use 100K POTS as shown in the schematic below:







Note that pin 3 out drives U2's reset (not trig in) pin 4 for enabling \ inhib. The switching frequency oscillator.

C12

U1 IGBT GATE Driver:

U1's output drives the IGBT GATE; it provides the duty cycle timing which is adjusted (at a given PRF) to maximize I in the primary of T1. The circuit at the right illustrates the 555 configured as a monostable oscillator. The high output state time is given:

 $t = 1.1 R_{A}C$

Using the same value C as for U2 (0.01 μ f) and assuming t < T of U2 then: (a) 50Khz => t = 20 μ sec : (a) 10Khz t = 100 μ sec

then @ 50khz $R_A = \sim 2K$; @ 10khz $R_A = \sim 10k$; the circuit for U1 is:

If VR1 is adjusted to 0 then $R_A = 2.2K \Rightarrow -50$ khz; if VR1 is set @ max. 10k then $R_A = 12.2K \Rightarrow f \sim <10$ khz.

The trigger input sets the internal 555 RS flip-flop causing C6 to discharge. If the trig. input doesn't pulse then pin 3 out could remain high causing Q1 to stay on and quickly overheat and burn out. To prevent this from happening the trigger signal from U2 is capacitor coupled to pin 2; R4 provides the pull up.

Pin 5 is shunted AC wise to GND with C9 to prevent noise spikes entering and causing pre-triggering.



